REMARKS

The present application has pending claims 1-12. No amendments were made to these claims nor were any new claims added.

In the Office Action the Examiner rejected claims 1-12 under 35 USC §102(e) as being anticipated by Ikeda (U.S. Patent Application Publication No. 2003/0023909 A1). This rejection is traversed for the following reasons. Applicants submit that the features of the present invention as recited in claims 1-12 are not taught or suggested by Ikeda whether taken individually or in combination with any of the other references of record.

The present invention is directed to a turbo encoder, turbo decoder and a radio base station which incorporates the turbo encoder and turbo decoder which operates in a manner so as to avoid outputting read addresses at which no data exists on a memory and implement an interleave read address generator or a deinterleave write address generator which has a circuit size smaller than other such conventional circuits. More particularly, the present invention provides, for example, a turbo decoder having an interleave address generator which sets an offset based on previously determined thresholds in accordance with symbol numbers generated by a counter. According to the present invention, this feature can avoid outputting read addresses at which no data exist on a memory and implements and interleave read address generator or a deinterleave write address generator having a circuit size smaller than such conventional circuits.

To accomplish the above the present invention provides that the interleave address generator adds an offset to a symbol number for the interleave input

sequence for correction and converts the corrected symbol number for the interleave input sequence to generate the read address when an address for randomly reading the interleave input sequence stored in the interleave memory exceeds the number of bits resulting from a subtraction of tail bits from the number of information bits of the interleave input sequence.

Alternatively, the present invention implements the above described features by providing that the interleave address generator converts a symbol number corresponding to an input symbol sequence to an address in accordance with a unique address conversion method to generate an interleave address and corrects the symbol number in accordance with a previously determined rule and converts the correct symbol number to generate the interleave address when the address converter from the symbol number does not match a previously set symbol number.

The above described features of the present invention now more clearly recited in the claims are not taught or suggested by any of the references of record whether taken individually or in combination with each other.

Particularly, the above described features of the present invention are not taught or suggested by Ikeda. Ikeda provides an interleave address generator which, when prime interleave addresses are generated, is capable of reducing processing load of generating interleave patterns. The Examiner's attention is directed to paragraph [0107] of Ikeda. This objective of the apparatus taught by Ikeda is entirely different from that of the present invention.

As per the above, the present invention is intended to avoid outputting read addresses at which no data exist on a memory and to implement an interleave read

address generator or a deinterleave write address generator in a circuit having a smaller size than that of conventional circuits. Thus, clearly the present invention is directed to solving a problem entirely different from the problem to which Ikeda is intended to solve.

Ikeda specifically provides an apparatus, for example, as illustrated in Figs. 7, 8, 11 and 12 wherein calculating means is provided for referencing a row transposition pattern value corresponding to the row number output from the row counter, multiplying means the reference row transposition pattern value by the number of columns of the matrix, thereby calculating an address offset value, and adding means for referencing the column transposition pattern value corresponding to the memory address granted by the memory address generating means, adding up the reference column transposition pattern value and the address offset value and generating an interleave address. Attention is directed to claim 5 of Ikeda.

The present invention differs entirely from that described above with respect to Ikeda. In contrast, the present invention provides that output addresses are obtained sequentially by counting up the input counter according to a predetermined law. In the present invention when there is a rule that when the output value is out of the threshold value, the counter is incremented to perform re-calculation, the offset (correct value) is added to the symbol in advance and the symbol thus added with the object is converted to obtain a read address, thereby avoiding outputting read addresses at which no data exist and further avoiding the increase of the calculation time due to the re-calculation of the read address and hence reducing the circuit size

as compared with conventional technique. Such features are clearly not taught or suggested by Ikeda.

Thus, Ikeda fails to teach or suggest an interleave address generator for generating write addresses for storing the interleaver input sequence in the interleaver memory and read addresses for randomly reading an interleaver input sequence stored in the interleaver memory wherein the interleave address generator adds an offset to a symbol number for the interleaver input sequence for correction, and converts the corrected symbol number for the interleaver input sequence to generate the read address when an address for randomly reading the interleaver input sequence stored in the interleaver memory sees the number of bits resulting from a subtraction of tail bits from the number of information bits of the interleaver input sequence as recited in the claims.

Therefore, as is quite clear from the above, the features of the present invention as clearly recited in the claims are not taught or suggested by Ikeda whether taken individually or in combination with any of the other references of record. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw the 35 USC §102(e) rejection of claims 1-12 as being anticipated by Ikeda.

The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the reference utilized in the rejection of claims 1-12.

In view of the foregoing amendments and remarks, Applicants submit that claims 1-12 are in condition for allowance. Accordingly, early allowance of claims 1-12 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (500.40552X00).

Respectfully submitted,

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